

## ABSTRACT OF THE DISCLOSURE

An improved binary decoder incorporating a selection circuit that activates a selected output corresponding to a input binary value, and a deselecting circuit coupled to each output that deactivates all other outputs when the selected output is activated. The deselecting circuit arrangement has a single input connected to the selected output and a plurality of outputs each of which is connected to one of the remaining outputs and forces them to the inactive state whenever the selected output is activated.

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